WHAT IS CLAIMED IS:

1. A wafer for use in a chip device comprising:

a. a non-passivated wafer;

b. a first titanium layer;

c. a first copper layer above the first titanium layer;

d. a second titanium layer above the first copper layer; and

e. a second copper layer above the second titanium layer.

2. A wafer in accordance with claim 1 further comprising a plurality of solder bumps.

3. A chip device comprising a wafer, the wafer comprising:

a. a non-passivated wafer;

b. a first titanium layer;

c. a first copper layer above the first titanium layer;

d. a second titanium layer above the first copper layer; and

e. a second copper layer above the second titanium layer.

4. A method of preparing a wafer for use in a chip device, the method comprising:

providing a non-passivated wafer;

depositing a first titanium layer on the non-passivated wafer;

depositing a first copper layer on the first titanium layer;

depositing a second titanium layer on the first copper layer; and

depositing a second copper layer on the second titanium layer.

5. A method of making a bumped wafer, the method comprising:

providing a non-passivated die;

alternatingly sputtering a first titanium layer, a first copper layer, a second titanium layer and a second copper layer onto the die;

depositing photo resist material onto the second copper layer;

etching isolation areas thereby removing the photo resist material, the second copper layer, the second titanium layer and the first copper layer at the isolation areas;

depositing photo resist material to define bump locations;

etching bump locations thereby removing the second copper layer and the second titanium layer at the bump locations

depositing under-bump material at the bump locations;

depositing solder on the under-bump material;

removing the photo resist material

etching away the second titanium layer at the isolation locations;

etching away the remaining second copper layer; and

reflowing the solder.